Enhanced Pulse-Density-Modulated Power Control for High-Frequency Induction Heating Inverters

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***Abstract*—This paper presents a 100-kW 100-kHz insulated-gate bipolar transistor (IGBT) series resonant inverter for induction heating applications that uses an improved power control scheme based on the standard pulse density modulation (PDM). This standard power control is a good solution for the design of high-frequency inverters because the output power factor is near to unity in a wide range of output power, resulting in great reduction of switching losses and electromagnetic noise. However, the output current can be in discontinuous mode, particularly for resonant loads of low quality factor or for low output power or low-load operation. This output current fluctuation produces a high output current ripple that can lead to an increase in power losses and loss of accuracy of the response of the frequency tracking control. The proposed control strategy, which is called enhanced PDM (EPDM), provides twice less output current ripple, thus resulting in an improved inverter behavior in terms of frequency tracking accuracy and energy efficiency. Experimental tests have been made, in order to compare the EPDM strategy with standard power control schemes.**

***Index Terms*—Induction heating (IH), pulse-density-modulation (PDM) power control, resonant power conversion.**

I. Introduction

INDUCTION HEATING (IH) generators are resonant inverters in which the resonant tank is formed by the heating coil and a series capacitor, in series resonant inverters (SRI) [1]–[3], or a parallel capacitor, in parallel resonant inverters (PRI) [4], [5]. They are used to heat metals to be welded, melted, or hardened [6], [7].

The use of SRIs that are fed with a voltage source represents a cost-effective solution; however, it does not have the ability to control the output power by itself when a simple control circuit is used, so that the output power of such an inverter has to be controlled by adjusting the dc input voltage. A thyristor bridge rectifier having input inductors and a dc-link capacitor has conventionally been used as a variable dc-voltage power supply. This causes some problems in size and cost. In order to overcome these problems, inverters with power control by frequency variation (FV) [7], pulsewidth modulation (PWM) [8], or phase-shift variation (PS) [9] are normally used to regulate the output power and using a single diode bridge rectifier as a dc voltage source.

This type of inverter regulates the output power by adjusting the frequency, pulsewidth, or phase shift of output voltage pulses, and no other power regulation circuit is needed. These power control schemes, however, may result in an increase in switching losses and electromagnetic noise because it is impossible to switch devices under both zero-voltage switching (ZVS) and zero-current switching (ZCS) conditions. Therefore, in high-frequency IH applications, MOSFET inverters must be used. Nevertheless, insulated-gate bipolar transistors (IGBTs) are preferred in high-power industrial applications (availability, cost, etc.), but their use is only possible if a low-loss power control scheme is found. In addition, these inverters are unsuitable for light load because the inner freewheeling current produces additional conduction losses and even more switching power losses.

Pulse-density-modulation (PDM) control technique results in simplification and reduction of constraints [10], [11]. Indeed, when applying this control scheme to an SRI, it is possible to eliminate the switching losses. The PDM control technique is suitable for high-frequency IH systems in the case of high-quality-factor (Q) loads, where the current fluctuations due to the ripple introduced by the power regulation are reduced. However, when the time constant of the load is not so high to make the output current continuous or under light load condition when the PDM modulation index is low, the duration of the passive mode of the inverter (when the freewheeling inverter current is quickly smoothed and reaches zero value) is too large, and then, the frequency tracking circuit cannot work normally. In this paper, we consider a novel PDM control method, which we have called enhanced PDM (EPDM), to reduce the output current ripple and to improve the control precision of the inverter.

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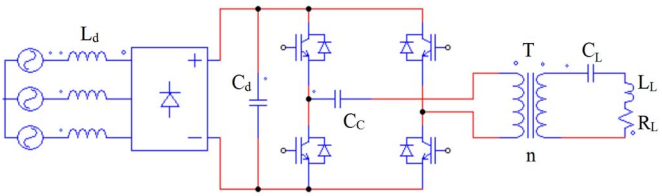

Fig. 1. System configuration.

This paper describes an IH system of 100 kW, 100 kHz, for industrial applications, that uses this novel low-loss control scheme. The working frequency is automatically adjusted close to the resonance frequency, in order to allow a quasi-ZCS mode, because the transistors are always turned off at low values of current. The blanking time of the inverter transistors is designed to maintain ZVS mode [8]–[11]. The EPDM output power control proposed in this work maintains this condition under a wide range of the output power. With this control scheme, an improvement in the inverter efficiency is also expected.

This paper is organized as follows: Section II presents the system configuration; Section III analyzes the EPDM inverter, shows the modulation principle and the switching pattern, and provides the equations to calculate the output power and the current ripple of the inverter, making a comparison with the standard PDM. Section IV describes the selected control of the inverter, and Section V validates the previous calculations using experimental data and gives a comparative analysis where the output current ripple and the energy efficiency of the inverter are measured for different control strategies. Finally, the conclusions are drawn.

II. System Configuration

Fig. 1 shows the typical system configuration of a series converter for IH. The output power stage consists of a single-phase voltage-source full-bridge inverter using four IGBT modules. The output of the inverter is connected to a series resonant circuit, composed by C_L and the IH loads (heating coil and workpiece) that can be modeled by means of a series combination of its equivalent resistance R_L and inductance L_L [12], [13]. The matching transformer T adapts the impedance of the load circuit. C_d is the dc-link capacitor, and C_C is an ac coupling capacitor. The dc power supply for the inverter is a three-phase diode bridge rectifier connected to the 400-V 50-Hz power line through the inductance L_d. The working frequency is 100 kHz, the maximum root-mean-square (RMS) value of the output voltage is 480 V, the maximum peak amplitude of the output current is rated to 300 A, and the maximum output power is 100 kW. The values of the main components of the circuit are shown in Fig. 1, where the given Q factor is approximately 11.

III. Analysis of the EPDM Inverter

A. Principle of EPDM

Fig. 2 shows the EPDM pattern compared with the PDM for similar output power level. The left row in Fig. 2 shows the switching pattern of the standard PDM inverter. The inverter

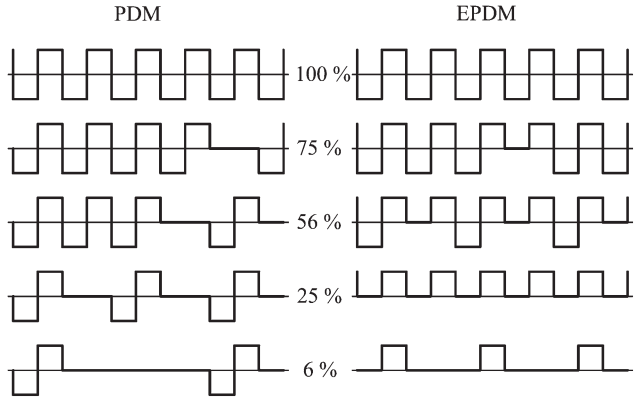

Fig. 2. Comparison between PDM and EPDM patterns for different values of inverter output power.

acts in two modes, i.e., the active mode, when the inverter acts as a square-wave voltage source with the amplitude of V_d for some resonant cycles, and the passive mode, when it acts as a zero-voltage source for some cycles. Note that the periodical repetition of this pattern determines a period T that is an integer multiple of the switching period T_s. The RMS value of the output voltage is proportional to the pulse density m that is the ratio of the duration of active mode T_{on} and the period T of the PDM cycle. In any case and to make a fair comparison of EPDM and PDM, we propose a PDM pulse distribution, which presents the minimum current ripple. When the output voltage is between 50% and 100%, the passive mode duration is one full switching period, while for voltages between 0% and 50%, now the active mode is one switching period. This work sequence can be described using the following equation:

$$\langle T \rangle = \begin{cases} \frac{T_S}{m} & 0 \leq m \leq 0,5 \\ \frac{T_S}{1-m} & 0,5 \leq m \leq 1 \end{cases} \quad (1)$$

where $\langle T \rangle$ is the average value of T for a large time. Thus, it is possible to control the output power of the inverter adjusting the pulse density.

The right row in Fig. 2 shows the EPDM pattern. For EPDM, the duration of the passive mode is half of a switching period. Note that making the new freewheeling cycle infinite, the minimum RMS value of output voltage is only half of the maximum value (25% of the output power). Therefore, after this RMS value, the definition of the freewheeling time must be the same as in the standard PDM. We will demonstrate in the following paragraphs that this control strategy permits to reduce the output current ripple.

Fig. 3 shows the idealized schematic diagram of the inverter circuit, where the transformer T has been removed and, hence, the impedances of the resonant circuit have been transformed by the turns ratio n. Q_1-Q_4 and D_1-D_4 are respectively the IGBT transistors and the freewheeling diodes that compose each power module. $V_{g1}-V_{g4}$ are the gate signals of the transistors, and C_1-C_4 represent the equivalent capacitance of the inverter switches, including the snubbing capacitor and the output capacitance of the IGBTs. We will suppose that all these capacitances have the same value C_S. The capacitor C_C, which needed to avoid the dc component of the output voltage,

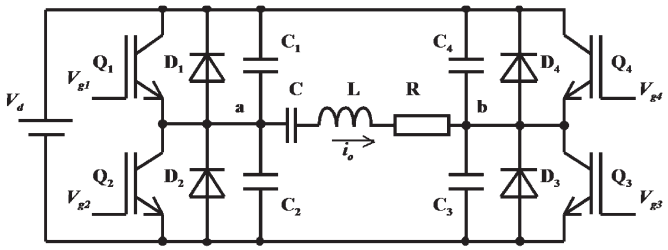

Fig. 3. Schematic diagram of the inverter.

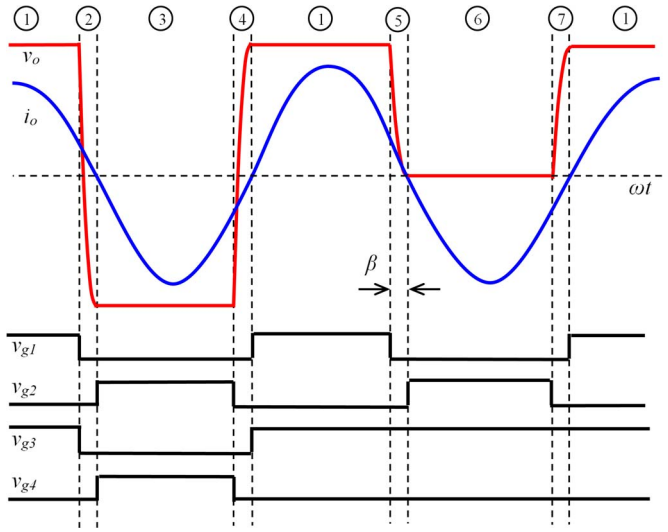

Fig. 4. Simplified output voltage and current waveforms for $P > 25\%$.

is removed from the circuit because its value is much larger than the resonant capacitor.

Fig. 4 shows the simplified gate signals and output voltage and current waveforms of the inverter, when the output power is larger than 25% and the duration of passive mode is half of the switching period. In the active mode, the four transistors Q_1–Q_4 are operated with almost 50% duty cycle. The switches in each leg of the bridge are turned on and off approximately (except the blank time) 180° out of phase. It operates above resonance, and the load current i_o lags the quasi-square-wave voltage v_o.

The phase portion β, when the output voltage is decreasing from positive to negative and the output current is positive, is essential to determine the ZVS operation. A mathematical expression for the value of β is required to know when ZVS is achieved. The expression can be calculated from the following charge analysis [10]: the current in the resonant circuit must be large enough to change the voltage in the switching capacitor C_S down to $-V_d$ (or up to $+V_d$) in the time β/ω just before the output current crosses zero. From these charge relations, β can be calculated as follows:

$$\beta = \cos^{-1}\left(1 - \frac{2\omega_S C_S V_d}{I_o}\right) \tag{2}$$

where $\omega_S = 2\pi f_s$, V_d is the voltage of the dc link, I_o is the amplitude of output current i_o, and f_S is the inverter switching frequency.

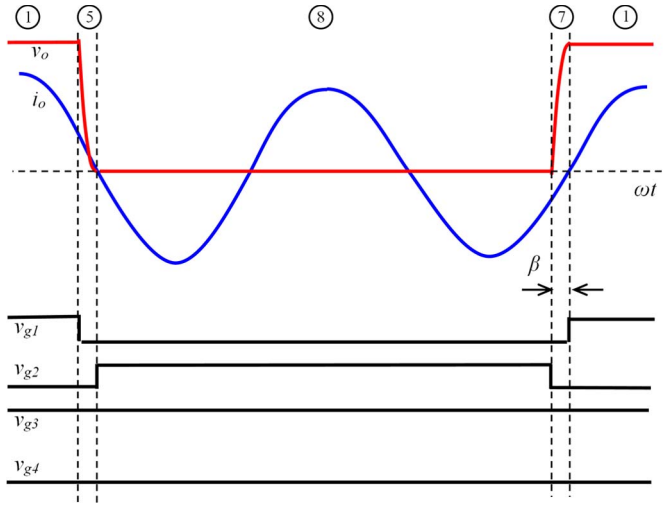

Fig. 5. Simplified output voltage and current waveforms for $P < 25\%$.

Fig. 5 shows the same signal when the output power is less than 25%. In the active mode, Q_1 and Q_3 conduct current from the dc power supply to the load, and in the rest of the EPDM period, the current is freewheeling. In this case, the definition of β is the same as in (2).

Fig. 6 shows the complete switching sequence of the EPDM inverter. The steps of the switching sequence are identified by the same numbers that are used in Figs. 4 and 5, and the inverter schematic corresponding to each step is shown. The current-carrying devices are drawn with solid lines, and the voltage-blocking devices are drawn with dotted lines. The direction of the current and the voltage polarity obtained at the end of each step has been expressed with arrows and ± signs or 0. The big arrows indicate the sequence flow beginning from step 1 that represents an active mode with positive current. For power larger than 25%, the next step is step 2 (ZVS) and step 3, where an active mode with negative current is represented. The active mode cycle is closed after the next ZVS process in step 4. The passive mode is inserted in the flow when step 1 is followed by the ZVS in step 5, step 6 to produce a zero-voltage state at its output terminals and step 7 (ZVS) to come back to the initial step 1. When power is less than 25%, the active mode is only present for positive current in step 1, and after the ZVS of step 5, the passive mode is carried out in step 8.The EPDM cycle is closed after the next ZVS in step 7.

B. Analysis of the Output Power of the EPDM Inverter

Fig. 7 shows a possible work situation of the EPDM inverter that must be considered only similar to an example that helps us to analyze the output power. The next equations will be valid for each different cycle of both EPDM and PDM power modulations only changing initial and final values of voltages and currents.

Since the frequency selectivity of a resonant circuit is large for IH application, if the frequency f of the square-wave voltage at the output of the inverter is very close to the resonant frequency f_o, only its first harmonic must be considered

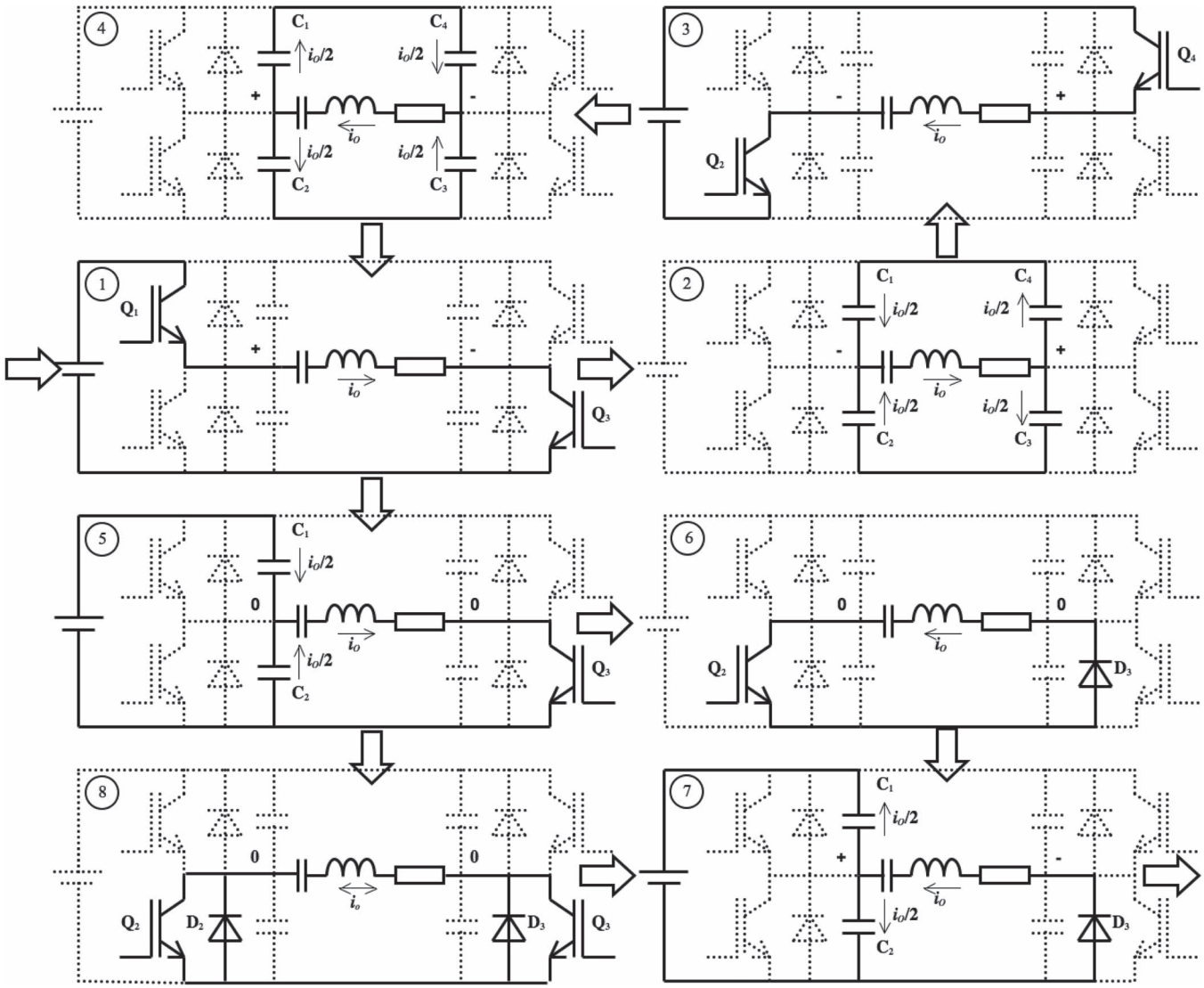

Fig. 6. Complete switching sequence of the EPDM inverter.

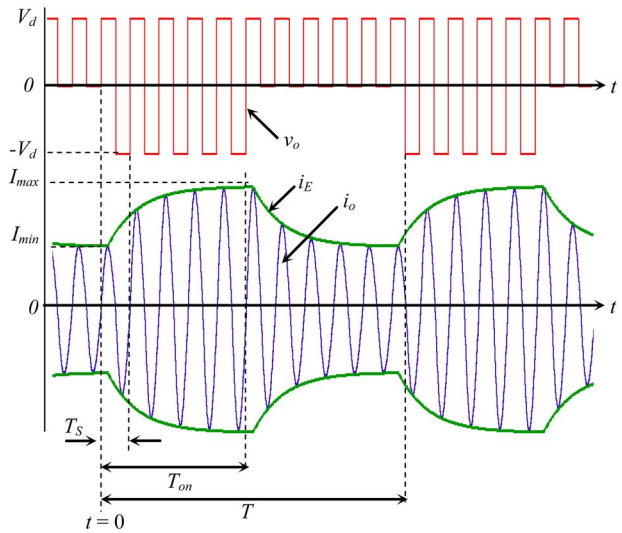

Fig. 7. Voltage and current waveforms in the EPDM inverter.

for power calculations. Under these conditions, we can apply Kirchhoff's voltage law to obtain the following equation [10]:

$$V_o \sin \omega_o t - L\frac{di_o}{dt} - \frac{1}{C}\int i_o dt - i_o R = 0 \tag{3}$$

where V_o is the amplitude of harmonic voltage, i_o is the current of the resonant circuit, and $\omega_o = 2\pi f_o = 1/\sqrt{LC}$.

Assuming that the quality factor of the series resonant circuit is $Q = L\omega_o/R \gg 1$, the output current of the inverter i_o is given by

$$i_o = i_E \sin(\omega_o t - \varphi) \tag{4}$$

where φ is the phase shift between the main harmonics of the output voltage and the output current.

The green line in Fig. 7 shows the envelope of the resonant current i_E that exhibits the first-order response of (4) with a

time constant given by

$$\tau = \frac{2L}{R} = \frac{2Q}{\omega_o}. \tag{5}$$

Therefore, i_E is given by

$$i_E = \begin{cases} I_{\max}\left(1 - e^{-\frac{t}{\tau}}\right) + i_E(0)e^{-\frac{t}{\tau}}, & 0 \le t \le T_{\text{on}} \\ i_E(T_{\text{on}})e^{-\frac{t-T}{\tau}} + I_{\min}\left(1 - e^{-\frac{t-T}{\tau}}\right), & T_{\text{on}} \le t \le T \end{cases} \tag{6}$$

where

$I_{\max}$ maximum current in case of $T_{\text{on}}/T = 1$;
$I_{\min}$ minimum current in case of $T_{\text{on}}/T = 0$;

$$i_E(0) = \frac{I_{\max}\left(e^{-\frac{T-T_{\text{on}}}{\tau}} - e^{-\frac{T}{\tau}}\right) + I_{\min}\left(1 - e^{-\frac{T-T_{\text{on}}}{\tau}}\right)}{1 - e^{-\frac{T}{\tau}}} \tag{7}$$

$$i_E(T_{\text{on}}) = \frac{I_{\max}\left(1 - e^{-\frac{T_{\text{on}}}{\tau}}\right) + I_{\min}\left(e^{-\frac{T_{\text{on}}}{\tau}} - e^{-\frac{T}{\tau}}\right)}{1 - e^{-\frac{T}{\tau}}}. \tag{8}$$

If the time constant is infinite, the amplitude of the resonant current is proportional to the pulse density

$$\lim_{\tau\to\infty} i_E = \frac{I_{\max}T_{\text{on}} + I_{\min}(T - T_{\text{on}})}{T}. \tag{9}$$

In the opposite case, when the time constant is very small, the current becomes a discontinuous waveform

$$\lim_{\tau\to 0} i_E = \begin{cases} I_{\max} & 0 \le t \le T_{\text{on}} \\ I_{\min} & T_{\text{on}} \le t \le T. \end{cases} \tag{10}$$

The active output power is obtained as follows:

$$\begin{aligned} P &= \frac{1}{T}\int_0^T v_o i_o \, dt \\ &= \frac{1}{T}\int_0^T V_o \sin\omega_o t \cdot i_E \sin(\omega_o t - \varphi)\, dt \\ &= \frac{1}{2T}\cos\varphi \int_0^T V_o i_E(t)\, dt. \end{aligned} \tag{11}$$

The amplitude of the output voltage V_o takes two different values $V_{\max}$ and $V_{\min}$, depending on the operation mode of the EPDM inverter. Hence, the output current amplitudes are

$$I_{\max} = \frac{V_{\max}}{|Z|} = \frac{V_{\max}}{R}\cos\varphi; \quad I_{\min} = \frac{V_{\min}}{|Z|} = \frac{V_{\min}}{R}\cos\varphi. \tag{12}$$

If $T \ll \tau$, the amplitude of the output current (9) is proportional to T_{on}/T; thus, the output power is given by

$$\lim_{\tau\to\infty} P = \frac{\cos^2\varphi}{2R}\left[\frac{(V_{\max} - V_{\min})T_{\text{on}} + V_{\min}T}{T}\right]^2. \tag{13}$$

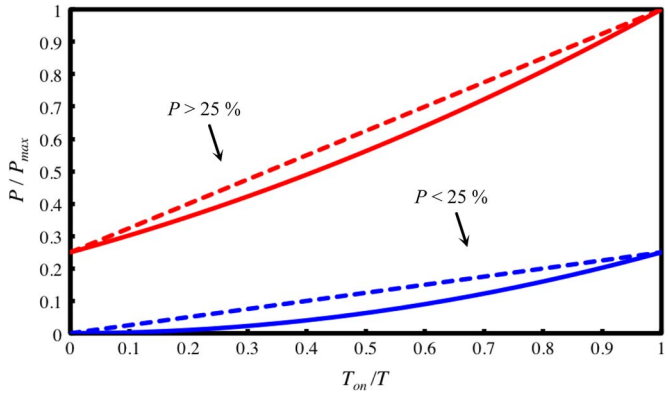

Fig. 8. Theoretical limits of the ratio between normalized output power and the EPDM pulse density.

If $T \gg \tau$, the output voltage and current become discontinuous waveforms, and the output power can be written as

$$\lim_{\tau\to\infty} P = \frac{\cos^2\varphi}{2R}\frac{V_{\max}^2 T_{\text{on}} + V_{\min}^2(T - T_{\text{on}})}{T}. \tag{14}$$

If output power is larger than 25%, the parameters $V_{\max}$ and $P_{\max}$, which are defined for $T_{\text{on}} = T$, and $V_{\min}$, for $T_{\text{on}} = 0$, are given by

$$V_{\max} = \frac{4V_d}{\pi}, \quad V_{\min} = \frac{2V_d}{\pi}, \quad P_{\max} = \frac{8V_d^2\cos^2\varphi}{\pi^2 R}. \tag{15}$$

Therefore, the output power value must be inside of the limits calculated in (13) and (14) as follows:

$$\frac{P_{\max}}{4}\left(1 + \frac{T_{\text{on}}}{T}\right)^2 \le P \le \frac{P_{\max}}{4}\left(1 + \frac{3T_{\text{on}}}{T}\right). \tag{16}$$

In the other case, when output power is less than 25%, $V_{\max}$ and $V_{\min}$ are given by

$$V_{\max} = \frac{2V_d}{\pi}; \quad V_{\min} = 0 \tag{17}$$

and the inverter output power is in the range of

$$\frac{P_{\max}}{4}\left(\frac{T_{\text{on}}}{T}\right)^2 \le P \le \frac{P_{\max}}{4}\left(\frac{T_{\text{on}}}{T}\right). \tag{18}$$

Fig. 8 shows the graphic representation of (16), in the right traces, and (18), in the left traces. Dashed lines represent the limits corresponding to low values of τ, and solid lines are valid when τ tends to infinity. Note that, in this way, it is possible to regulate the output power in the full range.

C. Analysis of the Output Current Ripple of the EPDM Inverter

The maximum peak-to-peak value of the output current ripple is obtained by the following expression:

$$\begin{aligned} \Delta I &= i_E(T_{\text{on}}) - i_E(0) \\ &= (I_{\max} - I_{\min})\frac{1 + e^{-\frac{T}{\tau}} - e^{-\frac{T_{\text{on}}}{\tau}} - e^{-\frac{T-T_{\text{on}}}{\tau}}}{1 - e^{-\frac{T}{\tau}}}. \end{aligned} \tag{19}$$

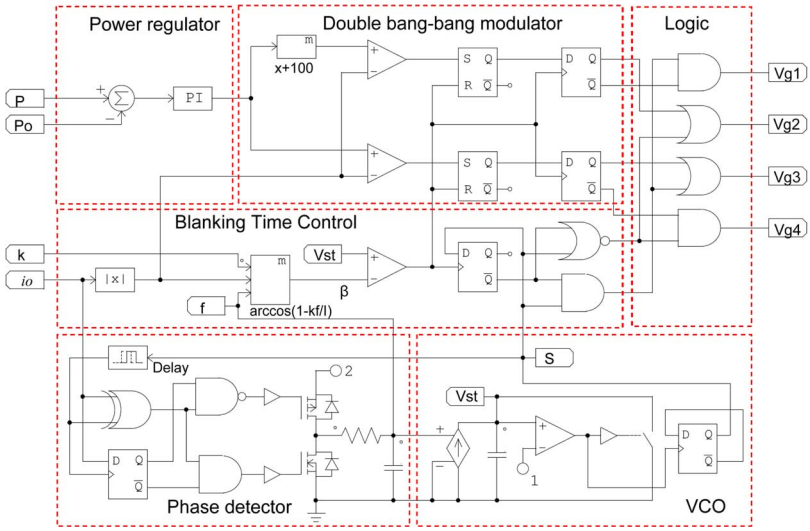

Fig. 9. Diagram of the control circuit.

Note that this equation is valid for any case of both EPDM and PDM inverters. In EPDM, $I_{\min} = I_{\max}/2$, for output power levels larger than 25%, and in PDM, $I_{\min} = 0$. If the output power is less than 25%, $I_{\min} = 0$ for both control strategies, but for EPDM, $I_{\max}$ is half of the value found in PDM. The quantity $(I_{\max} - I_{\min})$ is half for EPDM, and therefore, the obtained output current ripple can be divided by two.

The frequency of the output current ripple f_r that is the inverse of the EPDM period, can be obtained from (1). That is,

$$f_r = \begin{cases} f_s \frac{T_{\text{on}}}{T}, & 0 \le T_{\text{on}} \le T/2 \\ f_s \left(1 - \frac{T_{\text{on}}}{T}\right), & T/2 \le T_{\text{on}} \le T. \end{cases} \tag{20}$$

The largest ripple frequency is $f_r/2$ when $T_{\text{on}} = T/2$. For high values of quality factor Q, this happens in PDM when the output power is 25% of maximum output power. In EPDM, there are two maximums for output power 6% and 56%.

D. Balancing of the Output Voltage and Power Device Losses

The switching sequence presented in Section III-A causes an unbalanced pattern in the inverter output voltage. Fig. 2 shows that the average value of the EPDM inverter output voltage has a positive component in all cases, except when the output power is 100%. The extreme case is when output power is 25%, where the dc value of the output voltage is half of inverter input voltage V_d. It is because the IGBT transistors that are acting as active half-bridge (Q_1 and Q_2) are always the same. This results in dc voltage at the inverter output and unbalance of the IGBT switching and conduction losses. The first effect can be solved, including the dc decoupling capacitor C_C in series with the primary of the output transformer, but the second effect has not been solved. The solution for both effects can be letting both half-bridges work alternatively for each EPDM period. When the transistors that are acting like active half-bridge are Q_1 and Q_2, they have the most of the inverter power losses, and the dc value at the inverter output must be positive. In the next EPDM cycle, the active half-bridge must be composed by Q_3 and Q_4 that have the most of the power losses. Now, the dc inverter output voltage is negative. In this alternating operation, the average value of the output voltage will be near zero, and the capacitor C_C can be removed or minimized. Moreover, the losses of the all power devices of the inverter will be balanced. A possible balancing control strategy was shown in [11].

IV. Control Circuit

The control circuit designed to implement this EPDM inverter is a load-adaptive variable frequency system [14]–[16] that must be able to perform ZVS, under all operating conditions, and to generate the switching sequence discussed earlier. Fig. 9 shows a simplified diagram of the proposed control circuit. Since the phase detector and the voltage-controlled oscillator (VCO) act like a phase-locked loop, the signal S will be in phase with the inverter output current i_o. This signal S determines the rising slope of the trigger signal of the inverter transistors and, therefore, defines its turn-on switching. The delay block is used to compensate the time delay of the trigger signal from its generation in the control circuit until the effective switching off the transistors.

The blanking time indicates the time interval between the turn-off and turn-on switching of the transistors of the same leg. The blanking time control circuit generates the signal that references the turn-off switching of all transistors of the inverter, taking into account the calculation of (2), in order to achieve ZVS operation like shown in steps 2, 4, 5, and 7 in Fig. 6. For this calculation, we need the value of the amplitude of i_o, the value of the switching frequency that is obtained from the input of the VCO, and the value of the product of the dc-link voltage V_d and the equivalent output transistor capacitance C_S that is included as a constant value in the input k. A proportional–integral (PI) circuit is used to regulate the inverter power. The output of this regulator inputs a special design of a double bang-bang modulator that generates the trigger signal pattern of the EPDM inverter. The logic circuit collects all these signals to generate the four gate signals of the inverter.

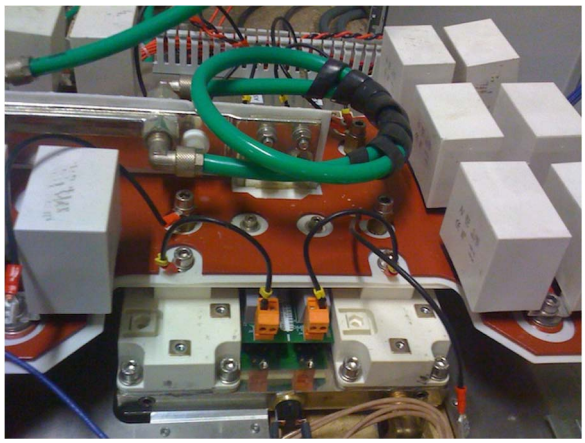

Fig. 10. Inverter view of the equipment under test.

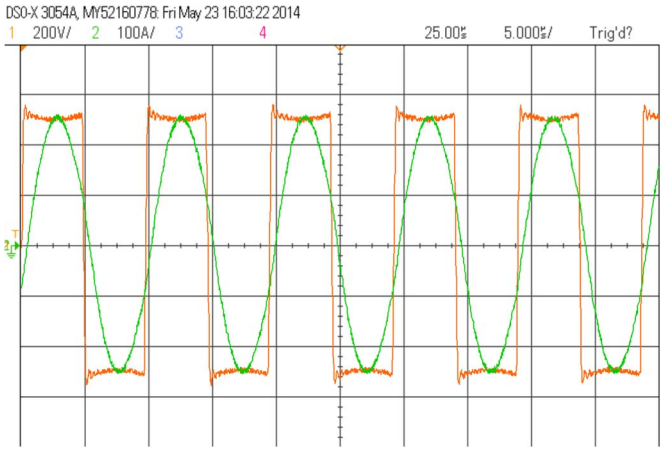

Fig. 11. Experimental waveforms of v_o (CH1) and i_o (CH2) of the EPDM inverter for 100% of the output power. (CH1: 200 V/div; CH2: 100 A/div; time base: 5 μs/div).

V. Experimental Results

The prototype described in Section III was tested, in order to meet the industrial application requests. The four IGBTs of the inverter (Eupec FZ600R12KS4) are rated at 1200 V and 600 A. For long time tests, a water-cooled dummy load was used. This load configuration represents a quality factor of approximately 11 that remained constant during all the tests. The experimental resonant frequency of the output circuit was 100.3 kHz. The control circuit automatically sets the switching frequency above the resonance that depends on the output power regulation due to the blanking time control.

A photograph of the experimental implementation of the inverter is shown in Fig. 10. This picture shows a detail of one of the two legs of the IGBTs of the inverter. Rectangular blocks are the dc-link capacitors placed at the sides of the picture; the snubber capacitors are placed on the small printed circuit boards (PCBs) between the transistor modules. The PCB of the driver circuit of the transistors was removed to show the water-cooled heat sinks of the transistors. The experimentally measured thermal resistance from the transistor junction to the water (ambient) is $R_{\mathrm{thJA}} = 0.05$ K/W. For all power measurements, a calorimetric method was used [18], [19].

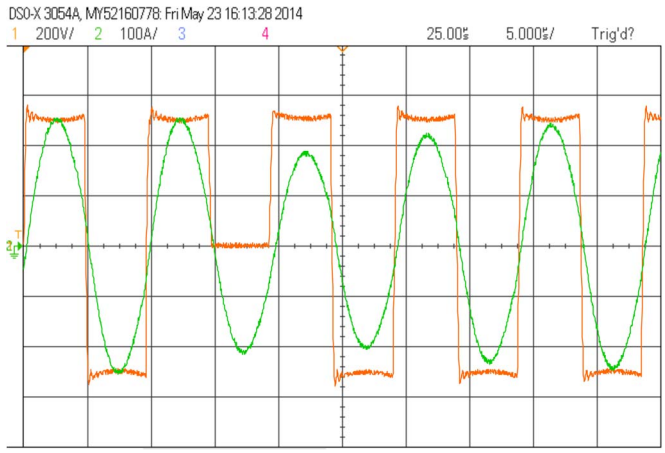

Fig. 12. Experimental waveforms of v_o (CH1) and i_o (CH2) of the EPDM inverter for 75% of the output power. (CH1: 200 V/div; CH2: 100 A/div; time base: 5 μs/div).

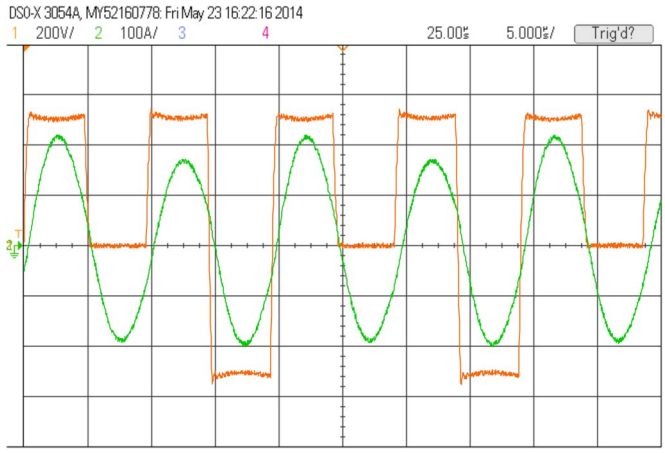

Fig. 13. Experimental waveforms of v_o (CH1) and i_o (CH2) of the EPDM inverter for 56% of the output power. (CH1: 200 V/div; CH2: 100 A/div; time base: 5 μs/div).

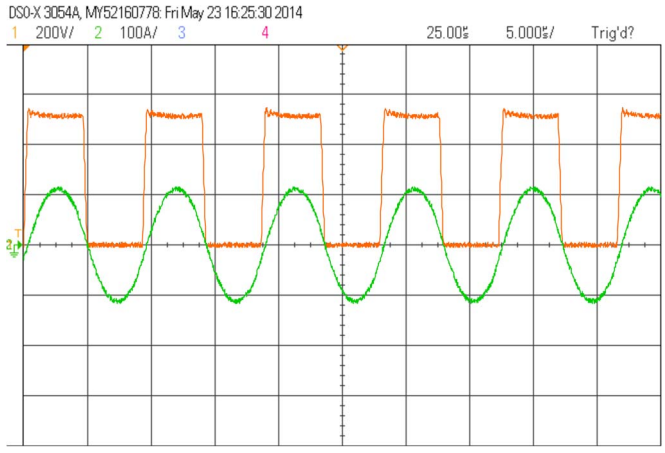

Fig. 14. Experimental waveforms of v_o (CH1) and i_o (CH2)) of the EPDM inverter for 25% of the output power. (CH1: 200 V/div; CH2: 100 A/div; time base: 5 μs/div).

Figs. 11–15 show experimental waveforms of the EPDM inverter output voltage v_o and the inverter output current i_o, for different output power levels that are approximately in the

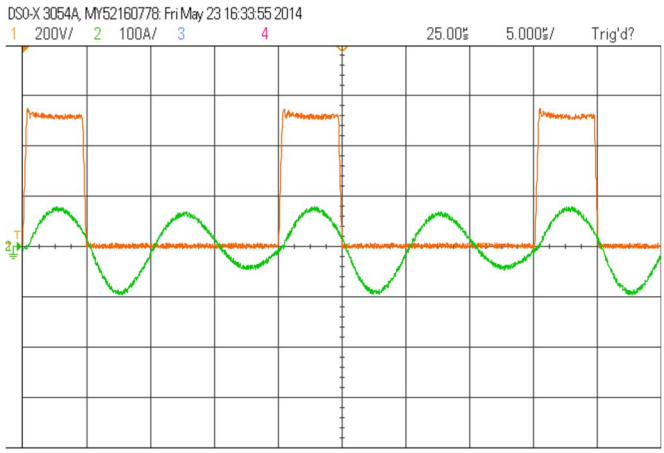

Fig. 15. Experimental waveforms of v_o (CH1) and i_o (CH2) of the EPDM inverter for 6% of the output power. (CH1: 200 V/div; CH2: 100 A/div; time base: 5 μs/div).

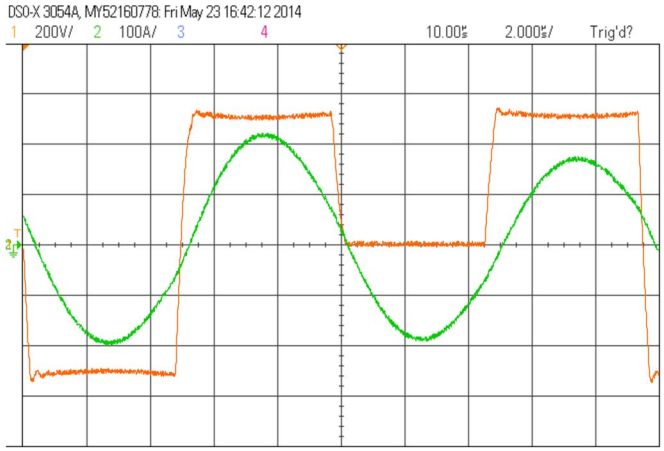

Fig. 16. Detail of the ZVS process. Experimental waveforms of v_o (CH1) and i_o (CH2) of the EPDM inverter for 56% of the output power. (CH1: 200 V/div; CH2: 100 A/div; time base: 2 μs/div).

range from 6 to 100 kW. These waveforms are similar to the ones shown in the right row in Fig. 2, and they demonstrate proper functionality of the designed power control circuit.

Fig. 16 shows with more detail the switching process, where it is possible to appreciate how the blanking time control circuit allows maintaining ZVS for all inverter transistors in active and in passive mode. The slopes of the output voltage reach their final value ($+V_d$, $-V_d$, or 0) just before the zero crossing of the output current.

A. Output Current Ripple

Tests made with this prototype allow also the validation of the calculations of the output current ripple. Fig. 17 shows the experimental waveforms of the inverter output voltage v_o and the inverter output current i_o for the same value of the output power (56%) that was shown in Fig. 13 but working in PDM mode. The measurement of the peak-to-peak ripple of the output current in both figures can demonstrate that the ripple of the EPDM inverter is half of the ripple of PDM.

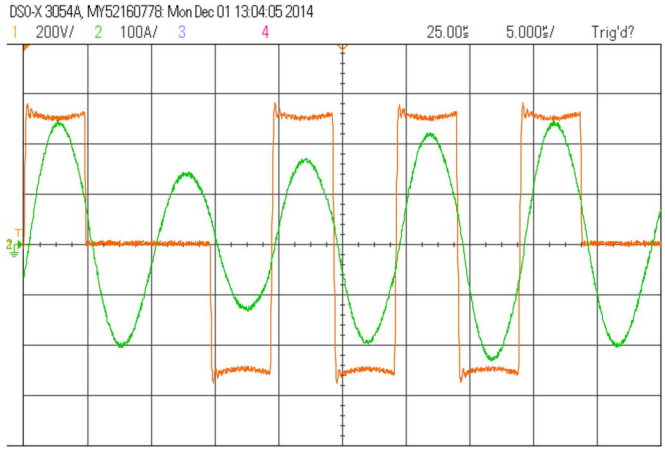

Fig. 17. Experimental waveforms of v_o (CH1) and i_o (CH2) of the PDM inverter for 56% of the output power. (CH1: 200 V/div; CH2: 100 A/div; time base: 5 μs/div).

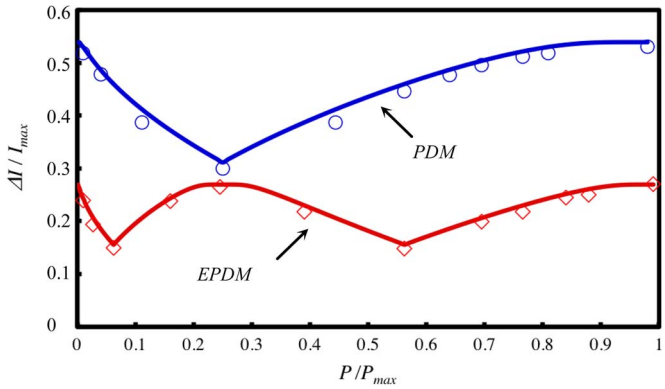

Fig. 18. Experimental comparison between EPDM and PDM output current ripple.

Fig. 18 presents the experimental results (circles and rhombus) and the theoretical calculation (19) of the normalized (with respect to the maximum value of output current) peak-to-peak current ripple of the EPDM inverter compared to the ripple of the PDM inverter for different values of the inverter output power. Note that the EPDM output current ripple is always less than the PDM ripple, and for output power levels higher than 56% and lower than 6%, the EPDM output current ripple is half of the PDM ripple.

B. Losses and Efficiency

In order to calculate the inverter efficiency, output power and total losses (switching and conduction) of the transistors and diodes must be measured. Power losses of the IGBTs have been measured using the calorimetric method applied to a water-cooled heat sink on top of which the power modules were mounted [17]–[19]. The relative error of this measurement was less than 5%. Losses of the passive component, bus bars, and cables have been estimated using approximate calculations.

A comparative study between the proposed EPDM versus PDM inverter has been made, in order to validate the theoretical calculations. This comparative study has been extended to other standard control strategies, such as the FV and the PS.

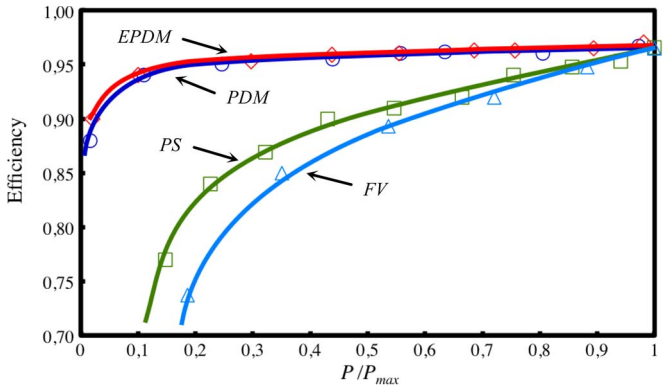

Fig. 19. Experimental inverter efficiency in function of normalized output power for different control strategies.

Fig. 19 shows the graphic representation of the inverter efficiency as a function of the normalized output power for the four control methods mentioned earlier.

For maximum output power, the efficiency is the same for all four control systems, but when the power decreases, the efficiency of FV and PS inverters falls rapidly due to the gradual reduction of the output power factor in the case of the FV regulation and the increase of the turn-off losses for both controls FV and PS. However, the PDM inverters work with a high efficiency over a wide range of output power because these types of inverters are able to keep ZVS and quasi-ZCS under any load condition. Additionally, we can notice that the efficiency of the EPDM inverter is slightly better than the efficiency of the standard PDM inverter because its lower current ripple makes better loss control.

Other working conditions were tested for different loads and output power levels, included slight load condition, and in any case, the behavior of the frequency tracking and the blanking time circuits was better in the EPDM inverter that in the PDM inverter.

VI. Conclusion

The purpose of this work was the development of an IGBT full-bridge inverter of 100 kW, 100 kHz based on a PDM control strategy, where the switching sequence was modified in order to improve its behavior under any output power level and load condition. The EPDM inverter is a cost-effective solution that incorporates the following improvements.

- The output power is regulated by varying the density of the voltage pulses in the inverter output following a novel switching sequence.
- The working frequency of the EPDM inverter does not depend on power regulation.
- EPDM control allows reducing twice the inverter output current ripple.
- EPDM inverter has the best efficiency of the tested inverters.
- The behavior of the electronic systems responsible for controlling the frequency tracking and the blanking time has been improved satisfactorily.

Comparing the experimental results and the calculations and simulations, the validity of the proposed inverter has been demonstrated.

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